Amendments to the Specification:

Please amend the title beginning on page 1, line 1 as follows:

LOCAL REGISTER INSTRUCTION FOR SELECTIVELY LOADING A REGISTER ~~MICRO ENGINE USED~~ IN A MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE

Please replace the paragraph beginning at page 11, line 11 with the following amended paragraph:

The "dest_reg" field represents an absolute or context-relative transfer register or general-purpose register (GPR) that holds the result of the instruction. The "byte_ld_enables" field represents a 4-bit mask that specifies which byte(s) are affected by the instruction. Each set bit enables the corresponding byte of the destination operand longword to be loaded or cleared. There must be at least 1 set bit in this mask. For example, 0101 loads the 1st and 3rd bytes while the other bytes remain unchanged. ~~In implementations, the bit mask can indicate a left shift n bits, where n is a number from one to thirty-one. The bit mask can indicate a left shift by an amount specified in a lower five bits of the first operand of a previous instruction, where the lower five bits is a number from one to thirty-one. The bit mask can indicate a right shift n bits, where n is a number from one to thirty-one. The bit mask can indicate a right shift by an amount specified in a lower five bits of the first operand of a previous instruction, where the lower five bits is a number from one to thirty-one. The bit mask can indicate a left rotate n bits, where n is a number from one to thirty-one. The bit mask can indicate a right rotate n bits, where n is a number from one to thirty-one.~~